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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/691,173      | 10/22/2003  | Yi-Nan Chen          | 10113081            | 6519             |

34283 7590 03/08/2005

QUINTERO LAW OFFICE  
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| EXAMINER |
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TRAN, MAI HUONG C

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| ART UNIT | PAPER NUMBER |
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2818

DATE MAILED: 03/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/691,173

Applicant(s)

CHEN ET AL.

Examiner

Mai-Huong Tran

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 February 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) 14-42 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restriction***

Application's election without traverse of Group I (Claims 1-13) drawn to a semiconductor device is acknowledged for prosecution in the subject application . Accordingly, claims 14-42 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

### **Specification**

The specification is objected to for the following reasons.

On page 3, line 25, TTO should be spelled out.

### **Claim Rejections - 35 U.S.C. § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6, 9-10, and 12-13 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,770,928 to Sommer et al.

Regarding to claim 1, Sommer discloses a memory device with vertical transistors and trench capacitors, comprising: a substrate 1, having at least one deep trench 5 therein; a trench capacitor 9, deposited in a lower position of the deep trench; a conducting structure 12, 13, 14, deposited on the trench capacitor, comprising a first conductive layer 13 and a second conductive layer 14; a ring shaped insulator 12, deposited on parts of the sidewall of the deep trench and between the substrate 1 of the deep trench and the first conductive layer 13, such that the first conductive 13 is surrounded by the ring shaped insulator 12, wherein the second conductive layer 14 is deposited on the first conductive 13 and the ring shaped insulator 12; a diffusion barrier 30, deposited on one side of the sidewall of the deep trench and between the second conductive layer 14 and the substrate 1 of the deep trench; a trench top isolation 32, deposited on the conducting structure; and a control gate 21, deposited on the trench top isolation 32 (col. 4, lines 3-67, col. 5, lines 1-48, and fig. 11).

Regarding to claim 2, the memory device further comprising: a buried strap 31, deposited within the substrate 1 beside parts of the conducting structure 12, 13, 14 where the diffusion barrier 30 is not deposited, serving as a source (col. 6, lines 10-16, and fig. 11).

Regarding to claim 3, the memory device further comprising: a doping area, provided within the substrate beside the control gate, serving as a drain (col. 1, lines 30-35).

Regarding to claim 4, the memory device wherein the ring shaped insulator comprises an oxide (col. 4, lines 53-56).

Regarding to claim 5, the memory device wherein the first conductive layer comprises a doped polysilicon or a doped amorphous silicon (col. 4, lines 57-60).

Regarding to claim 6, the memory device wherein the second conductive layer comprises a doped polysilicon or a doped amorphous silicon (col. 4, lines 66-67).

Regarding to claim 9, the memory device wherein the trench top isolation comprises an oxide (col. 5, lines 14-15).

Regarding to claim 10, the memory device wherein the control gate comprises a gate layer and a gate dielectric layer deposited between the gate layer and the substrate (col. 5, lines 31-32, lines 45-48, and fig. 11).

Regarding to claim 12, the memory device wherein the gate dielectric layer

comprises an oxide (col. 5, lines 32-33).

Regarding to claim 13, the memory device wherein the buried strap is electrically connected with the control gate and formed by diffusing dopants of the first conductive layer into the substrate of the trench surrounding the top of the second conductive layer (col. 5, lines 5-67, and col. 6, lines 1-21).

### **Claim Rejections - 35 U.S.C. § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 7 and 11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,770,928 to Sommer et al. in view of Cappelani et al. (6800898).

Regarding to claim 7, Sommer discloses the invention except for the memory device wherein the diffusion barrier comprises an oxide. However, Cappelani teaches the diffusion barrier comprises an oxide (col. 4, lines 20-23).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the diffusion barrier comprises an oxide, as taught by Cappelani in order to increase the packing density, it is advantageous if the second part of the conductive structure adjoins the region of the substrate on only one sidewall of the depression. In this case, depressions of different memory cells can be arranged at a small distance from one another without leakage current occurring between mutually adjacent conductive structures (col. 6, lines 59-65).

Regarding to claim 11, Sommer discloses the claimed invention except for the memory device wherein the gate layer comprises a polysilicon, a silicide, a metal layer, or a combination thereof. However, Cappelani teaches the gate layer comprises a polysilicon, a silicide, a metal layer, or a combination thereof (col. 1, lines 65-67, and col. 2, line 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory device wherein the gate layer comprises a polysilicon, a silicide, a metal layer, or a combination thereof, as taught by Cappelani in order to increase the packing density, it is advantageous if the second part of the conductive structure adjoins the region of the substrate on only one sidewall of the depression. In this case, depressions of different memory cells can be arranged at a small distance from one another without leakage current occurring between mutually adjacent conductive structures (col. 6, lines 59-65).

Claim 8 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,770,928 to Sommer et al. in view of the remark.

Regarding to claim 8, Sommer discloses the claimed invention except for the memory device wherein the thickness of the diffusion barrier is substantially less than 100 ANG. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the thickness of the diffusion barrier less than 100 ANG, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

### **Conclusion**

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published



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applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mai-Huong Tran



David Nelms  
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